

AMENDMENTS TO THE CLAIMS

A complete listing of the claims follows. Claims 1-22 are presently pending in this application, prior to entry of the following:

1. (original) A method of forming an array of non-volatile memory cells on a semiconductor substrate surface, comprising:
 - forming a plurality of shallow trench isolation structures spaced apart across the surface of a substrate in a first direction and extending in a second direction, individual shallow trench isolation structures having sidewalls that extend vertically from the substrate surface;
 - forming a plurality of floating gate structures, individual floating gate structures extending between a first sidewall of a first shallow trench isolation structure and a second sidewall of a second shallow trench isolation structure and being bounded in a first direction by the first and second sidewalls; and
 - shaping the plurality of floating gate structures to reduce the width in a second direction of an upper part of individual ones of the plurality of floating gate structures.
2. (original) The method of claim 1 further comprising forming a first plurality of masking portions extending in a first direction by the same step used to form the plurality of floating gates, the first plurality of masking portions extending over shallow trench isolation structures and over floating gate structures.
3. (original) The method of claim 2 further comprising forming a second plurality of masking portions having sidewalls in contact with ones of the first plurality of masking portions and subsequently removing the first plurality of masking portions.
4. (original) The method of claim 3 further comprising forming a plurality of sidewall spacers that are in contact with the sidewalls of the second plurality of masking portions and that extend over portions of the floating gate structures.

5. (original) The method of claim 4 further comprising forming a third plurality of masking elements, an individual one of the third plurality of masking elements extending between ones of the plurality of sidewall spacers on a floating gate structure and subsequently removing the plurality of sidewall spacers.
6. (original) The method of claim 5 wherein shaping the plurality of floating gate structures comprises etching the floating gate structures with the plurality of masking elements in place.
7. (original) The method of claim 1 further comprising forming a plurality of control gates that overlie the plurality of floating gate structures.
8. (original) The method of claim 7 wherein a control gate extends on either side of a shaped floating gate structure in the second direction.
9. (original) The method of claim 7 wherein a control gate extends on one side of a shaped floating gate structure in the second direction.
10. (original) The method of claim 7 wherein a control gate extends to enclose the upper part of a floating gate structure on three or four sides and from above.
11. (original) A method of forming an array of non-volatile memory cells on a semiconductor substrate surface, comprising:
 - forming a plurality of structures having sidewalls that extend from the substrate surface;
 - forming a plurality of conductive strips, an individual conductive strip extending between a first sidewall and a second sidewall of the plurality of structures having sidewalls, an individual conductive strip bounded by the first and second sidewalls;
 - forming a plurality of separate floating gate structures by removing portions of the plurality of conductive strips, removed portions extending from a first sidewall to a second sidewall;

then forming a plurality of masking elements, an individual masking element covering a portion of one of the plurality of floating gate structures; and

then etching the plurality of floating gate structures to remove portions of the floating gate structures that are not covered by masking elements.

12. (original) The method of claim 11 further comprising etching back the plurality of structures having sidewalls prior to forming a plurality of masking elements.

13. (original) The method of claim 11 wherein the individual masking element extends over part of an upper surface and part of two side surfaces of the one of the plurality of floating gate structures.

14. (original) The method of claim 11 wherein an individual floating gate structure has an upper surface and a lower surface that are parallel to the substrate surface, the removed portions extending from the upper surface to a level that is between the upper surface and the lower surface.

15. (original) A method of forming an array of non-volatile memory cells on a semiconductor substrate surface, comprising:

forming a first plurality of conductive strips that are separated in a first direction, that extend across the substrate surface in a second direction and that have protrusions extending in a direction away from the substrate surface with recesses between protrusions;

forming a dielectric layer overlying the first plurality of conductive strips;

forming a conductive layer over the dielectric layer; and

etching portions of the conductive layer and the first plurality of conductive strips in the same pattern to form a second plurality of conductive strips from the conductive layer, the second plurality of conductive strips extending in a first direction, and to form a plurality of floating gates from the first plurality of conductive strips, an individual floating gate having at least a portion of a protrusion and at least a portion of a recess, an individual conductive strip overlying the at least a portion of a protrusion and the at least a portion of a recess of a floating gate.

16. (original) The method of claim 15 wherein a portion of the individual conductive strip extends into the at least a portion of a recess of a floating gate.
17. (original) The method of claim 15 wherein the at least a portion of a protrusion has a surface that extends along a first plane that is perpendicular to the substrate surface, the individual conductive strip has a surface that extends along a plane that is parallel to the first plane and is separated from the first plane by the dielectric layer.
18. (original) The method of claim 15 wherein etching removes half of a protrusion and half of a recess.
19. (withdrawn) A floating gate memory cell on a substrate surface, comprising:
a floating gate having a first floating gate portion and a second floating gate portion;
the first floating gate portion bounded by a first shallow trench isolation structure and a second shallow trench isolation structure in a first direction and extending between a first side and a second side in a second direction that is perpendicular to the first direction;
the first floating gate portion having a lower surface that extends across the substrate surface and an upper surface parallel to the lower surface, the upper surface bounded in the second direction by a first edge and a second edge; and
the second floating gate portion extending from the upper surface of the first floating gate portion, the second floating gate portion extending equally with the first floating gate portion in the first direction and having a first surface that extends from the first edge of the upper surface and a second surface that extends from a line on the upper surface that is between the first edge and the second edge.
20. (withdrawn) The memory cell of claim 19 further comprising a conductive gate that overlies the floating gate, the conductive gate having a first side that is coplanar with the first surface of the second floating gate portion and a second side that is coplanar with the second side of the first floating gate portion.

21. (withdrawn) The memory cell of claim 20 wherein the second floating gate portion covers a part of the upper surface of the first floating gate portion and leaves a part of the upper surface uncovered and the conductive gate overlies both the second floating gate portion and the uncovered part of the upper surface.

22. (withdrawn) The memory cell of claim 20 wherein the control gate has a surface that extends across the second surface of the second floating gate portion.